IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Anthony Richard Bonaccio et al.
Serial No.	:	09/682,473
Filed	:	September 6, 2001
For	:	CLOCK SIGNAL DISTRIBUTION UTILIZING DIFFERENTIAL SINUSOIDAL SIGNAL PAIR
Examiner	:	An T. Luu
Group Art Unit	:	2816

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF

Dear Sir:

Appellants hereby appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner in the Final Office Action dated March 26, 2003, rejecting claims 1-42.

REAL PARTY IN INTEREST:

The present application is assigned to International Business Machines Corporation, New Orchard Road, Armonk, New York 10504.

RELATED APPEALS AND INTERFERENCES:

No other appeals or interferences are known to the Appellants, to the Appellants' legal representative, or to the Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF THE CLAIMS:

Claims 8 and 13 are pending, claims 1-7, 9-12 and 14-42 having been canceled without prejudice in an amendment filed concurrently. Both claims 8 and 13 are independent claims.

Claims 8 and 13 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,184,736 (hereinafter "Wissell et al.") in view of U.S. Patent No. 5,448,188 (hereinafter "Matsumoto et al.").

STATUS OF AMENDMENTS:

An amendment filed concurrently with the present appeal brief and canceling claims 1-7, 9-12 and 14-42 without prejudice awaits entry by the Examiner. No amendments relative to claims 8 or 13 have been filed.

SUMMARY OF THE INVENTION:

In at least one embodiment of the invention, a signal generator 10 (FIG. 1) generates a differential sinusoidal signal pair. A differential sinusoidal signal pair comprises a pair of sinusoidal wave forms, that are substantially equal in frequency and amplitude but that are substantially 180° out of phase with each other. (Appellants' Specification paragraph 18). The distribution circuitry 12 distributes the differential sinusoidal signal pair from the signal generator 10 to points on an integrated circuit at which local clock signals are to be generated. (Appellants' Specification paragraph 20). Coupled to the distribution circuitry 12 are clock receivers 16. The purpose of the clock receivers 16 is to receive the differential sinusoidal signal pair distributed through the distribution circuitry 12 and to convert the differential sinusoidal signal pair to local clock signals having a suitable wave form and amplitude. (Appellants' Specification paragraph 24).

Since a differential sinusoidal signal pair is used for distributing the clock signal, very low-swing signals may be

employed, thereby greatly economizing on power consumption. Moreover, since local clock signal regeneration is performed on a differential basis with reference to the distributed pair of signals, noise which couples to both of the pair of signals is automatically filtered out. Also, since the clock signal is sinusoidal prior to regenerating, its energy is concentrated at the clock frequency rather than being spread through the spectrum as in the case of a square wave clock signal. Consequently, energy efficiency is promoted. (Appellants' Specification paragraph 11).

ISSUES:

1. Whether claims 8 and 13 are unpatentable under 35 U.S.C. §103(a) over Wissell et al. in view of Matsumoto et al.

GROUPING OF THE CLAIMS:

Claims 8 and 13 relate to Issue 1. No other claims are being appealed.

ARGUMENTS:

ISSUE 1

35 U.S.C. 103(a) Rejection of Claims 8 and 13

The final rejection of claim 8 under 35 U.S.C. 103 is improper because neither Wissell et al. nor Matsumoto et al. alone or in combination, disclose, teach or suggest a method of driving a clock tree on an integrated circuit (IC) that includes the steps of:

(a) providing an IC having a clock tree;

(b) distributing a clock signal in the form of a

differential sinusoidal signal pair in a portion of the clock tree, the differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

(c) generating a local clock signal from the differential pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal.

as required by claim 8. The final rejection of claim 13 under 35 U.S.C. 103 is improper because neither Wissell et al. nor Matsumoto et al. alone or in combination, disclose, teach or suggest a clock circuit for an IC that includes:

(a) a generating circuit adapted to generate a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

(b) a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

(c) a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals by employing both the first sinusoidal signal and the second sinusoidal signal to form each local clock signal.

as required by claim 13. In addition, the Examiner has improperly combined the relied upon references because there is no teaching, suggestion or motivation for such a combination found in the references themselves or in the knowledge generally

available to one of ordinary skill in the art. In failing to identify such a teaching, suggestion or motivation, the Examiner has failed to establish a *prime facie* case of obviousness. For these reasons, Appellants respectfully request that the Examiner's final rejection of claims 8 and 13 be reversed and that claims 8 and 13 be allowed.

The Wissell et al. reference discloses a clock generation circuit that generates radio-frequency sinusoidal signals. The radio-frequency signals are distributed over dedicated clock lines to clock users. (Column 2, lines 10-14 and FIG. 3). It is noted that the circuitry disclosed in the Wissell et al. reference does not employ both sinusoidal signals received as inputs to the receiver chip shown in FIG. 3 to generate either of the digital clock signals output from the receiver chip of FIG. 3. Specifically, the "digital SIN clock signal" is formed only from the "SIN" sinusoidal input, and the "digital COS clock signal" is generated only from the "COS" input sinusoidal signal. In contrast, claim 8 specifically requires generating a local clock signal from the differential pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal. Likewise, claim 13 specifically requires clock receiver circuits that are adapted to convert the differential sinusoidal signal pair into respective local clock signals by employing both the first sinusoidal signal and the second sinusoidal signal to form each local clock signal.

Paragraph 18 of Appellants' specification defines the term "differential sinusoidal signal pair" as "a pair of sinusoidal wave forms, that are substantially equal in frequency and amplitude but that are substantially 180° out of phase with each other" (Emphasis added). It is noted that this definition is consistent with the conventional understanding of the term "differential sinusoidal signal pair". Appellants note that generation of a differential sinusoidal signal pair, as so defined and claimed, and generation and distribution of a clock

signal therefrom, are not disclosed or suggested by the Wissell et al. reference. In the portion of its disclosure that is most nearly relevant to the present invention, the Wissell et al. reference discloses, at column 5, lines 6-10, "a phase splitter 42...for producing clock signals at phases that are 90° apart, i.e. quadrature-related clock signals". Thus the plural clock signals generated in Wissell et al. are 90° apart, not 180° apart, as is the case of the claimed differential sinusoidal signal pair. In other words, quadrature related clock signals, as disclosed in Wissell et al. are different from a "differential sinusoidal signal pair" as recited in claims 8 and 13 and defined in the specification.

The Matsumoto et al. reference discloses a "signal processing device for selectively producing as an output signal either a signal corresponding to an input signal" or "a signal which may be a fixed voltage level for muting purposes or a mixed signal". (Abstract). Appellants respectfully urge that the Matsumoto et al. reference has nothing to do with generating a clock signal, as recited in claim 8. As explained in columns 1 and 2 of the Matsumoto et al. reference, the general subject of the reference is circuitry for muting or mixing video signals. Moreover, the circuit of FIG. 1 of the Matsumoto et al. reference, upon which the Examiner appears to rely, is for selectively muting an input signal (see column 6, lines 3-6) and not for generating a clock signal.

To go into further detail, there is not the slightest indication in the discussion of FIG. 1 of the Matsumoto et al. reference that the output signal Vout of the circuit shown in FIG. 1 is to be used as a clock signal. Rather, in a non-muting operation mode of the circuit, the signal Vout corresponds to the input signal Vin (column 5, lines 46-49) and accordingly is an information signal such as a brightness component of a video signal. When the circuit of FIG. 1 is in a muting operation

mode, the output signal Vout is a constant level.[1] Thus, the output signal Vout of the circuit of FIG. 1 of the Matsumoto et al. reference is either a video signal component or a constant voltage level, neither of which is a clock signal for an integrated circuit. It follows that the Matsumoto et al. reference completely fails to disclose the claim limitation of "generating a local clock signal...." of claim 8 or converting "the differential sinusoidal signal pair into respective local clock signals by employing both the first sinusoidal signal and the second sinusoidal signal to form each local clock signal" of claim 13.

As the Examiner states, the Wissell et al. reference fails to disclose a receiver circuit that outputs a single clock signal as required by claims 8 and 13 (e.g., by employing both first and second signals of the differential pair). (Office Action of March 26, 2003, page 3, paragraph 2). However, the Examiner states that "it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching" of the Matsumoto et al. reference (FIG. 1) into that of the Wissell et al. reference because "a receiver circuit can be implemented in many different ways to accommodate the requirement of particular application." The Examiner further states that a "skilled artisan in the art would have been motivated to combine these references to produce a stabilized clock output signal by mixing corresponding of a plurality of input signals.". (Office Action of March 26, 2003, page 3, paragraph 2).

As provided in relevant part by MPEP § 2143.01, "obviousness can only be established by ... modifying the teachings of the prior art to produce the claimed invention wherein there is some teaching, suggestion or motivation to do so found either in the references themselves or in the knowledge

[1] See column 5, lines 65-68, which indicates that "Vout becomes Vcc - I2 x R1". Since each of Vcc, I2 and R1 are constants, Vout must also be a constant. See also column 6, lines 14-15.

generally available to one of ordinary skill in the art." Moreover, MPEP §2142 states that "[t]he tendency to resort to 'hindsight' based on the applicant's disclosure is often difficult to avoid due to the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of facts gleaned from the prior art."

It appears that the Examiner has arrived at the proposed modification of the Wissell et al. reference by using the current application itself as a template. As stated above, the Matsumoto et al. reference has nothing to do with generating a clock signal. The output signal Vout of the circuit of FIG. 1 of the Matsumoto et al. reference is either a video signal component or a constant voltage level, neither of which is a clock signal for an integrated circuit. Accordingly, because the Matsumoto et al. reference has nothing to do with generating a clock signal, and in fact does not generate a clock signal, Appellants respectfully submit that the only motivation to combine the Wissell et al. reference with the Matsumoto et al. reference is Appellants' specification. Appellants respectfully submit that such use of hindsight reasoning to formulate a rejection is improper as per MPEP §2142.

MPEP §2143 further provides that "[i]f [a] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." Contrary to this requirement, it is apparent that essential functions of the apparatus of the Wissell et al. reference would be destroyed if the apparatus were modified as suggested by the Examiner. For example, and as stated above, the signals generated in Wissell et al. (FIG. 2) are 90° apart, not 180° apart, as is the case of the claimed differential sinusoidal signal pair. Further, the circuitry disclosed in the Wissell et al. reference does not employ both sinusoidal signals received as

inputs to the receiver chip shown in FIG. 3 to generate either of the digital clock signals output from the receiver chip of FIG. 3. The Wissell et al. reference employs quadrature signals to generate (1) the "digital SIN clock signal" formed only from the "SIN" sinusoidal input; and (2) the "digital COS clock signal" formed only from the "COS" input sinusoidal signal. It is unclear how the Wissell et al. reference could be modified to employ the Matsumoto et al. circuit (which employ differential sinusoidal inputs not quadrature inputs) and still achieve its intended purpose of generating two clock signals that are 90° out of phase. Appellants respectfully submit that the proposed modification would render the prior art invention being modified (Wissell et al.) unsatisfactory for its intended purpose, and as such, that there is no suggestion or motivation to make the proposed modification.

Finally, as stated above, the output signal Vout of the circuit of FIG. 1 of the Matsumoto et al. reference is either a video signal component or a constant voltage level, neither of which is a clock signal for an integrated circuit. Accordingly, even if the Wissell et al. reference could be modified to include the circuitry of Matsumoto et al., such a combination would not generate a local clock signal from the differential pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal as required by claim 8; or to convert the differential sinusoidal signal pair into respective local clock signals by employing both the first sinusoidal signal and the second sinusoidal signal to form each local clock signal as required by claim 13.

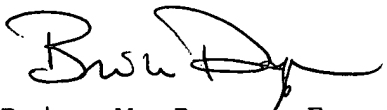
Conclusion

As demonstrated above, each of claims 8 and 13 recites one or more limitations not present in the relied-upon prior art and the Examiner's suggested combination is improper for multiple reasons. First, there is no motivation to combine the Wissell et

al. reference and the Matsumoto et al. reference as suggested by the Examiner. Rather, the Examiner has improperly combined/modified the relied upon references based on hindsight. Second, such a combination/modification would render the Wissell et al. reference unsatisfactory for its intended purpose. Third, such a combination/modification would not produce Appellants' claimed invention. For at least these reasons, Appellants respectfully submit that the appealed claims are allowable over the prior art of record.

Please charge deposit account no. 04-1696 in the amount of $330.00 to cover the cost of filing Appellants' Brief, and $420.00 for the two-month extension fee. A separate Request for Two-Month Extension of Time is enclosed. Appellants do not believe any other fees are due regarding this Brief. However, if any additional fees are required, please charge deposit account no. 04-1696.

Respectfully Submitted,



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Tarrytown, New York

APPENDIX

8. A method of driving a clock tree on an integrated circuit (IC), the method comprising the steps of:

providing an IC having a clock tree;

distributing a clock signal in the form of a differential sinusoidal signal pair in a portion of the clock tree, the differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

generating a local clock signal from the differential pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal.

13. A clock circuit for an IC, comprising:

a generating circuit adapted to generate a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals by employing both the first sinusoidal signal and the second sinusoidal signal to form each local clock signal.